SHRI JAGDISHPRASAD JHABARMAL TIBREWALA UNIVERSITY

श्री जगदीशप्रसाद झाबरमल टीबडेवाला विश्वविद्यालय

Department of Electronics and Communication Engineering

Scheme and Syllabus

(2013-2015)

M.Tech.(Microelectronics and VLSI Design)

Scheme and Syllabus for

[Microelectronics and VLSI Design] (MVD)

Semester-1st

Sr. No.	Name of Subject	Subject Code	Internal Theory Exam		External Theory Exam		
			Max. Marks	Min. Passing Marks	Max. Marks	Min. Passing Marks	Total Marks
1	**Physics of Semiconductor Devices**	**MMV-101**	30	12	70	28	100
2	**Microelectronic Technology IC Fabrication**	**MMV-102**	30	12	70	28	100
3	**Digital VLSI Design**	**MMV-103**	30	12	70	28	100
4	**System Design using HDLs**	**MMV-104**	30	12	70	28	100
5	**System Design using HDLs Lab**	**MMV-105**	40	16	60	24	100
6	**Digital VLSI Design Lab**	**MMV-106**	40	16	60	24	100
			Total				**600**

Semester-2nd

Sr. No.	Name of Subject	Subject Code	Internal Theory Exam		External Theory Exam		
			Max. Marks	Min. Passing Marks	Max. Marks	Min. Passing Marks	Total Marks
1	**Analog Integrated Circuit Design**	**MMV-201**	30	12	70	28	100
2	**VLSI Sensor Technology and MOEMS**	**MMV-202**	30	12	70	28	100
3	**Embedded Systems**	**MMV-203**	30	12	70	28	100
4	VLSI Signal Processing	**MMV-204.1**	30	12	70	28	100
5	Process & Device Characterization & Measurements	**MMV-204.2**	30	12	70	28	100
6	Low Power Design Techniques	**MMV-204.3**	30	12	70	28	100
7	**Analog Integrated Circuit Design Lab**	**MMV-205**	40	16	60	24	100
8	**Embedded Systems Lab**	**MMV-206**	40	16	60	24	100
			Total				**600**

Semester-3rd

Sr. No.	Name of Subject	Subject Code	Internal Theory Exam		External Theory Exam		
			Max. Marks	Min. Passing Marks	Max. Marks	Min. Passing Marks	Total Marks
1	VLSI Testing & Verification	**MMV-301.1**	30	12	70	28	100
2	VLSI Architectures	**MMV-301.2**	30	12	70	28	100
3	Nanoelectronics	**MMV-301.3**	30	12	70	28	100
4	Modeling for Submicron Devices	**MMV-302.1**	30	12	70	28	100
5	System-on-Chip (SOC) Design	**MMV-302.2**	30	12	70	28	100
6	High Speed Circuit Design	**MMV-302.3**	30	12	70	28	100
7	**Seminar**	**MMV-303**					100
8	**Thesis (starts i.e. Literature Review and Work Plan)**	**MMV-304**					200
			Total				**500**

Semester-4th

Sr. No.	Name of Subject	Subject Code	Internal Theory Exam		External Theory Exam		
			Max. Marks	Min. Passing Marks	Max. Marks	Min. Passing Marks	Total Marks
1	**Thesis Continu…**	**MMV-304**					**500**
		Grand Total					**2200**

Note: Elective subject will be run only when number of students for that subject will be minimum ten.

Note: One research paper published in referred journal is compulsory for all M.Tech.(MVD) students at the time of thesis submission.

MMV-101 PHYSICS OF SEMICONDUCTOR DEVICES

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UNIT-1 Semiconductor Electronics: Physics of Semiconductor Materials, Drift Velocity, Mobility, Scattering, Diffusion current Band Model. Metal Semiconductor Contacts: Metal-Semiconductor System, (V-I) and (C-V) equations for a Shottky - Barrier - Diode, Diode Construction, Device analysis using surface - states, applications as mixer and detectors in microwave region, Ohmic Contacts, Surface effects.

UNIT-2 PN Junctions: Step junction, Linearly Graded Junction, (V-I) and (C-V) characteristics, Junction Break-down, tunneling effect, avalanche multiplication, transient behaviour and noise, Use of junction diode as a rectifier, Voltage regulator, resistor varactor and fast recovery diode.

UNIT-3 Bipolar Junction Transistors: Transistor action, Current-Voltage equation, Output characteristics, Breakdown voltage, Ebers-Moll and Gummel-Poon Model, Early effect, Charge control model, small-signal transistor model, Simulation model.

UNIT-4 Metal-oxide-silicon System: MOS structure, Energy Band Diagrams, Interface charges, Surface effects, MOS Capacitors.

UNIT-5 MOS Transistors: Basic Theory, structure and operation, MOSFET parameters, Threshold Voltage and its control, Geometric effects on threshold, Ion-Implanted MOSFETs, Complementary MOSFET, Sub-threshold Conduction, Velocity saturation, Hot carriers, small geometry considerations.

Text Books:

1. Sze, S. M., Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons (1981).
2. Millman, J. and Halkias, C., Integrated Electronics, Tata McGraw Hill (1972).

Reference Books:

1. Muller, R. S. and Kamins, T. I., Device Electronics for Integrated Circuits, 3rd Edition, Wiley (2003).
2. Richman P., MOS Field Effect Transistor and Integrated Circuits, John Wiley & Sons (1973).

MMV-102 MICRO-ELECTRONIC TECHNOLOGY IC FABRICATION

L	T	P
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UNIT-1 Crystal Growth and Wafer Preparation: Electronic Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Processing Considerations.

UNIT-2 Epitaxy: Vapour Phase Epitaxy - basic transport processes and Reaction Kinetics, doping and auto-doping, equipments and safety considerations, buried layers, epitaxial defects, Molecular Beam Epitaxy - equipment used, film characteristics, SOI structures.

UNIT-3 Diffusion: Models of Diffusion in Solids, Fick's laws for diffusion, Measurement Techniques, Fast diffusion in Silicon, Diffusion in polycrystalline Silicon and SiO_2. Oxidation: Growth Mechanism and Kinetics, Silicon Oxidation Model, Interface Considerations, Orientation dependence of Oxidation Rates Thin Oxides. Oxidation Technique and Systems - Dry and Wet Oxidation, Plasma Oxidation, Masking Properties of SiO_2.

UNIT-4 Lithography: Optical Lithography - Optical resists, contact and proximity printing, projection printing, electron lithography - resists, mask generation, Electron Optics - Roaster scan and Vector scan, variable beam shape, X-ray lithography - Resists and Printing, X-ray sources and masks, Ion-Lithography.

UNIT-5 Etching: Reactive plasma etching, AC and DC plasma excitation, plasma properties, chemistry and surface interactions, feature size control and an isotropic etching, ion enhanced and induced etching, properties of etch processes. Reactive - Ion - Beam – Etching, Specific etch processes: PolySi/Polycide, Trench etching, SiO_2 & Si_3N_4. Sub-micron process techniques, ULSI Technology, Nano-fabrication.

Text Books:

1. Sze, S. M., VLSI Technology, Tata McGraw Hill (2003).
2. Plummer, J. D., Deal M. D. and Griffin P. B., VLSI Technology: Fundamentals, Practice, and Modeling, Prentice Hall (2000).

Reference Books:

1. Nagchodhari, D., Principles of Microelectronics Technology, A H Wheele (1998).
2. Gandhi, S. K., VLSI Fabrication Principles, 2nd Edition, John Wiley & Sons (2003

MMV-103 DIGITAL VLSI DESIGN

L	T	P
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UNIT-1 Physics and Modeling of MOSFETs: Basic MOSFET Characteristics – Threshold Voltage, Body Bias concept, Current-Voltage Characteristics – Square-Law Model, MOSFET Modeling – Drain-Source Resistance, MOSFET Capacitances, Geometric Scaling Theory – Full-Voltage Scaling, Constant-Voltage Scaling. Fabrication and Layout of CMOS Integrated Circuits: Overview of Integrated Circuit Processing – Oxidation, Photolithography, Self-Aligned MOSFET, Isolation and Wells – LOCOS, Trench Isolation, CMOS Process flow, Mask design and Layout – MOSFET Dimensions, Design Rules, Latch-up.

UNIT-2 CMOS Inverter: Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics – Switching Intervals, High-to-Low time, Low- to-High time, Maximum Switching Frequency, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.

UNIT-3 Switching Properties of MOSFETs: nMOSFET/ pMOSFET Pass Transistors, Transmission Gate Characteristics, MOSFET Switch Logic, TG-based Switch Logic, D-type Flip-Flop. Static CMOS Logic Elements: Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo- nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.

UNIT-4 Power Dissipation in CMOS Digital Circuits: Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current. Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families: Charge Leakage, Charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Multiple-Output Domino Logic, NORA Logic, Single-Phase Logic.

UNIT-5 Effects of Technology Scaling on CMOS logic styles: Trends and Limitations of CMOS technology scaling – MOSFET scaling trends, Challenges of MOSFET scaling – Short-Channel effects, Subthreshold Leakage currents, Dielectric Breakdown, Hot Carrier effects, Soft Errors, Velocity Saturation & Mobility Degradation, DIBL, Scaling down V_{dd}/V_{th} ratio. CMOS Differential Logic Styles: Dual-Rail Logic, CVSL, CPL, DPL, DCVS, MCML. Issues in Chip Design: ESD Protection, On-Chip Interconnects – Line Parasitics, Modeling of the Interconnect Line, Clock Distribution, Input-Output circuits.

Text Books:

1. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, 3rd Edition, Tata McGraw Hill (2003).
2. Weste, N. H. E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, 2nd Edition, Addision Wesley (1998).

Reference Books:

1. Rabaey, J. M., Chandrakasen, A. P. and Nikolic, B., Digital Integrated Circuits – A Design Perspective, 2nd Edition, Pearson Education (2003).
2. Baker, R. J., Lee H. W. and Boyce D. E., CMOS Circuit Design, Layout and Simulation, 2nd Edition, Wiley - IEEE Press (1997).
3. Weste, N. H. E., Harris, D. and Banerjee, A., CMOS VLSI Design, 3rd Edition, Pearson Education (2006).

MMV-104 SYSTEM DESIGN USING HDLs

L	T	P
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UNIT-1 Introduction: To HDLs and logic synthesis. Logic synthesis: design cycle, types of synthesisers, design testing and verification, design optimization techniques, technology mapping, VHDL design hierarchy, objects, types and sub-types, design organization, VHDL design cycle. RTL level design: RTL design stages, VHDL description of the RTL design.

UNIT-2 Combinational logic: Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignments, conditional signal assignments, selected signal assignment. Types: Synthesisable types, standard types, standard operators, scalar types, records, arrays, attributes.

UNIT-3 Operators: Standard operators, operator precedence, Boolean operators, comparison operators, arithmetic operators, concatenation operators. Package std_logic_arith: Std_logic_arith package, making the package visible, contents of std_logic_arith, resize functions, operators, shift functions, type conversions, constant values, mixing types in expressions, numeric packages. Sequential VHDL: Processes, signal assignments, variables, if statements, case statements.

UNIT-4 Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model of asynchronous reset, asynchronous reset templates, registered variables. Hierarchy: Role of components, using components, component instances, component declaration, Configuration specifications, default binding, binding process, component packages, generate statements.

UNIT-5 Sub programs: Functions, type conversions, procedures, declaring subprograms. Test benches: Test benches, verifying responses, clocks and resets, printing response values, reading data files, reading standard types, error handling. Libraries: Standard libraries, organising files, library names, library work, incremental compilation. Basic principles of Combinational logic design, sequential logic design, arithmetic circuit design and control logic design.

Text Books:

1. Naylor D. and Jones S., VHDL: A logic synthesis approach, Springer, 1997.
2. Rushton A., VHDL for Logic Synthesis, Wiley, 1998.

Reference Books:

1. Ashenden P., The Designer's Guide To VHDL, Morgam Koughman, 2007
2. Bhaskar J., A VHDL Primer, PEARSON / Prentice Hall, 2006

MMV-201 ANALOG INTEGRATED CIRCUIT DESIGN

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UNIT-1 Basic MOS Device Physics: MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, MOSFET Noise. Analog MOS Process: Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors & Resistors, Substrate Coupling, Ground Bounce.

UNIT-2 Single Stage Amplifiers: Common Source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode. Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell. Current Sources & Mirrors: Current Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

UNIT-3 Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers. Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References. Feedback: General Considerations, Topologies, Effect of Loading.

UNIT-4 Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR. Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques. Noise: Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

UNIT-5 Switched-Capacitor Circuits: Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback. Non Linearity and Mismatch: Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques, Reduction of Noise by Offset Cancellation.

Text Books:

1. Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (1999).
2. Gregorian, R. and Temes, G. C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (1986).

Reference Books:

1. Allen, P. E. and Holberg, D. R., CMOS Analog Circuit Design, 2nd Edition, Oxford University Press (2002).
2. Johns, D. A. and Martin, K., Analog Integrated Circuit Design, John Wiley (1997).
3. Gray, P. R., Hurst, P. J., Lewis, S. H., and Meyer, R. G., Analysis and Design of Analog Integrated Circuits, 4th Edition, John Wiley (2001).
4. Hastings, A., The Art of Analog Layout, Prentice Hall (2001).

MMV- 202 VLSI SENSOR TECHNOLOGY AND MOEMS

L	T	P
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UNIT-1 Introduction to MEMS: Overview of CMOS process in IC fabrication, MEMS system-level design methodology, Equivalent circuit representation of MEMS, Signal conditioning circuits and Sensor Noise calculation.

UNIT-2 Principles of Physical and Chemical Sensors: Sensor classification, Sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.

UNIT-3 Sensor Characterization and calibration: Study of Static and Dynamic Characteristics, Sensor Reliability, Aging Test, Failure Mechanisms and their evaluation and stability study.

UNIT-4 Sensor Modeling: Numerical modeling techniques, Model equations, different effects on modeling (mechanical, electrical, thermal, magnetic, optical, chemical and biological) and examples of modeling. Sensor Technology: Thick and Thin Films fabrication process, Micro machining, IOC (Integrated Optical Circuit) fabrication process, Wire Bonding and Packaging.

UNIT-5 Sensor Applications: Pressure Sensors with embedded electronics, accelerometer with transducer, gyroscope, RF MEMS Switch with electronics, Process engineering, medical diagnostic and patient monitoring, environmental monitoring. Future aspects of MEMS: RF MEMS, Optical MEMS, NEMS, MOEMS.

Text Books:

1. Mohamed Gad-el-Hak, MEMS: Introduction and Fundamentals, 2nd Edition, CRC Press (2005).
2. Maluf, N., An Introduction to Micro-ElectroMechnical Systems Engineering, Artech House (2000).
3. Ristic, L. (Editor), Sensor Technology and Devices, Artech House (1994).
4. Leondes, T. C., MEMS/ NEMS Handbook: Techniques and Application, 1st Edition, Springer Press (2006).

Reference Books:

1. Lyshevski, S. E., Nano- and Micro-Electromechanical Systems: Fundamentals of Nano- and Micro engineering, 2nd Edition, CRC Press (2005).
2. Santos, H. J. De Los, Introduction to Micro-Electro-Mechanical (MEM) Microwave Systems, Artech House (1999).
3. Ballantine, D. S., *et al.*, Acoustic Wave Sensors, Academic Press (1997).
4. Masoos Tabib-Azar, Microactuators, Kluwer (1998).
5. Allen, J., Micro Electro Mechanical System Design, CRC Press (2005).
6. Senturia, S. D., Microsystem Design, Kluwer (2001).

MMV-203 EMBEDDED SYSTEMS

L	T	P
3	1	1

UNIT-1 Embedded Processing: Introduction to Embedded Computing, Difference between Embedded and General-Purpose Computing, Characterizing Embedded Computing, Design Philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, Role of the Compiler, Architectural structures, The datapath, Registers and Clusters, Memory Architecture, Branch architecture, Speculation and prediction, Prediction in the embedded domain, Register File Design, Pipeline Design, the control unit, control registers.

UNIT-2 Embedded Processors: Microprocessor versus Microcontroller architecture, ARM architecture, Embedded Cores, Soft and Hard Cores, Architecture of Configurable Microblaze soft core, Instruction set, Stacks and Subroutines, Microblaze Assembly Programming, Input-Output interfacing, GPIO, LCD interfacing, Peripherals, DDR Memory, SDRAM, Microblaze interrupts, Timers, Exceptions, Bus Interfacing, DMA, On-chip Peripheral bus (OPB), OPB Arbitration, OPB DMA.

UNIT-3 RTOS and Application design: Programming language choices, Traditional C and ANSI C, C++ and Embedded C++, matlab, Embedded JAVA, Embedded C extensions, Real time operating systems, Embedded RTOS, Real time process scheduling, structure of real time operating system. Memory management in Embedded operating system, operating system overhead, interprocess communication mechanisms, File systems in Embedded devices, Different types of locks, Semaphores, Application studies with Vxworks, Montavista Linux etc

UNIT-4 System Design and Simulation: System-on-a-Chip (SoC), IP Blocks and Design Reuse, Processor Cores and SoC, Non-programmable accelerators, reconfigurable logic, multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing.

UNIT-5 Use of simulators, Compilers, Loaders, Linkers, locators, assemblers, Libraries, post run optimizer, debuggers, profiling techniques, binary utilities, linker script**,** system simulation, In Circuit Emulation, Validation and verification, Hardware Software partitioning, Co-design.

Text Books:

1. Wolf, W., High-Performance Embedded Computing Architectures, Applications, and Methodologies, Morgan Kaufman Publishers (2007).
2. Heath, S., Embedded Systems Design, Elsevier Science (2003).

Reference Books:

1. Fisher, J. A., Faraboschi, P. and Young, C., Embedded Computing - A VLIW Approach to Architecture, Compilers and Tools, Morgan Kaufman (2005).
2. Simon, D. E., An Embedded Software Primer, Pearson Education (2005).

MMV-204.1 VLSI SIGNAL PROCESSING

L	T	P
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UNIT-1 Introduction: Introduction to DSP Systems, Terminating and Non-Terminating, Representation of DSP programs, Data Flow graphs (DFGs), Single rate and multi rate DFGs, Iteration bound, Loop, Loop Bound, Iteration rate, Critical loop, Critical path, Area-Speed-Power trade-offs, Precedence constraints, Acyclic Precedence graph, Longest Path Matrix (LPM) and Minimum Cycle Mean (MCM) Algorithms, Pipelining and parallel processing of DSP Systems, Low Power Consumption.

UNIT-2 Algorithmic Transformations: Retiming, Cut-set retiming, Feed-Forward and Feed-Backward, Clock period minimization, register minimization, Unfolding, Sample period reduction, Parallel processing, Bit-serial, Digit-serial and Parallel Architectures of DSP Systems, Folding, Folding order, Folding Factor, Folding Bi-quad filters, Retiming for folding, Register Minimization technique, Forward Backward Register Allocation technique.

UNIT-3 Systolic Architecture Design and Fast Convoltuion: Systolic architecture design methodology, Projection vector, Processor Space vector, Scheduling vector, Hardware Utilization efficiency, Edge mapping, Design examples of systolic architectures, Cook-Toom Algorithm and Modified Cook-Toom Algorithm, Wniograd Algorithm and Modified Winograd Algorithm, Iterated Convolution, Cyclic Convolution.

UNIT-4 Algorithm Strength Reduction: Introduction, Parallel FIR filters, Polyphase decomposition, Fast FIR filters Algorithms, Discrete Cosine Transform and Inverse Discrete Cosine Transform, Algorithm-Architecture Transformation, DIT Fast DCT, Pipelined and Parallel Recursive and Adaptive Filters, Look-Ahead Computation, Look-Ahead Pipelining, Decompositions, Clustered Look-Ahead Pipelining, Scattered Look-Ahead pipelining, Parallel processing in IIR Filters, Combining Pipelining and Parallelism.

UNIT-5 Scaling and Round-off Noise: Introduction, State variable description of Digital Systems, Scaling and Round-off Noise Computation, Slow-Down Approach, Fixed-point digital filter implementation.

Text Books:

1. Parhi, K. K., VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley & Sons (1999).
2. Oppenheim, A. V. and Schafer, R. W., Discrete-Time Signal Processing, Prentice Hall (1999).

Reference Books:

1. Mitra, S. K., Digital Signal Processing. A Computer Based Approach, McGraw-Hill (2001).
2. Wanhammar, L., DSP Integrated Circuits, Academic Press (1999).

MMV-204.2 PROCESS AND DEVICE CHARACTERIZATION & MEASUREMENTS

L	T	P
3	1	0

UNIT-1 Physical Characterization: Thin Film Thickness- Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR.

UNIT-2 Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope. Material and Impurity Characterization: SIMS, XRD, EDAX.

UNIT-3 Electrical Characterization: Four-probe technique, Hall Effect, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements.

UNIT-4 Process and SPICE model parameter Extraction: SPICE BSIM3 model parameter extraction and optimization, Intrinsic Most and extrinsic, parasitic element, EKV model, Gummel-Poon model, BSIM model.

UNIT-5 Test Structures for Process Characterization: Contact Resistors, Split Cross Bridge Resistors, Self-aligned n+ Bridges. Test Structures for Device Characterization: Individual MOSFETs, 4x4 MOSFET Arrays, Capacitors. Test Structures for Faults and Reliability Analysis: Contact Chains, Serpentine/Comb Resistors.

Text Books:

1. Runyan, W. R. and Shaffner, T. J., Semiconductor Measurements and Instrumentation, 2nd Edition, McGraw-Hill (1998).
2. Schroder, D. K., Semiconductor Material and Device Characterization, 2nd Edition, Wiley (1998).

References Books:

1. Kane, P. F. and Larrabee, G. B., Characterization of Semiconductor Materials, Mc-Graw Hill (1970).
2. K.V. Ravi, Imperfections and Impurities in Semiconductor Silicon, John Wiley and Sons, (1981)

MMV-204.3 LOW POWER DESIGN TECHNIQUES

L	T	P
3	1	0

UNIT-1 Low Power Microelectronics: Retrospect and Prospect, Fundamentals of power dissipation in microelectronic devices, Estimation of power dissipation due to switching, short circuit, sub- threshold leakage, and diode leakage currents.

UNIT-2 CMOS Scaling: Scaling for High Performance and Low-Power.

UNIT-3 Low Voltage Technologies and Circuits: Threshold Voltage Scaling and Control, Multiple Threshold CMOS (MTCMOS), Substrate Bias Controlled Variable Threshold CMOS, Testing Issues: Design and test of low-voltage CMOS circuits.

UNIT-4 Circuit And Logic Styles: Power-conscious logic Styles, Adiabatic Logic Circuits. Power Analysis and optimization: Power Analysis Techniques, Power Optimization Techniques, Energy recovery techniques, Software power estimation and optimization Low-Power Memory Circuits and architectures.

UNIT-5 Power conscious high-level synthesis, Silicon-on-Insulator Based Technologies.

Text Books:

1. Roy, K. and Prasad, Sharat C., Low Power CMOS VLSI: Circuit Design, John Wiley & Sons (2000).
2. Chandrakasan, A. P. and Broderson, R. W., Low Power Digital CMOS Design, Kluwer (1995).

Reference Books:

1. Rabaey, J. M. and Pedram, M., Low Power Design Methodologies, Kluwer (1996).
2. Yeo, K. S. and Roy K., Low Voltage, Low Power VLSI Subsystems, McGraw-Hill (2004).
3. Sanchez-Sinencio, E. and Andreou, A. G., Low-Voltage/Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits, IEEE Press (1999).
4. Bellaouar, A. and Elmasry, M. I., Low-Power Digital VLSI Design: Circuits and Systems, Kluwer (1995).

MMV-301.1 VLSI TESTING AND VERIFICATION

L	T	P
3	1	0

UNIT-1 Physical Faults and their modeling; Stuck-at faults; Bridging Faults; Fault collapsing, Fault Simulation; Deductive, Parallel and Concurrent Fault Simulation; Critical Path Tracing.

UNIT-2 ATPG for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM; Random, Exhaustive and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

UNIT-3 PLA Testing: Cross Point Fault Model and Test Generation. Memory Testing: Permanent, Intermittent and Pattern Sensitive Faults; Marching Tests; Delay Faults.

UNIT-4 ATPG for Sequential Circuits; Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board level Testing; BIST and Totally Self Checking Circuits; System Level diagnosis. Introduction: Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes; Reconfiguration Techniques; Yield Modeling Reliability and effective area utilization.

UNIT-5 Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SoCs. Design verification techniques based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Text Books:

1. Abramovici, M., Breuer, M. A. and Friedman, A. D., Digital Systems Testing and Testable Design, Jaico Publishing House (2001).
2. Rashinkar, P., Paterson and Singh, L., System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic (2001).

Reference Books:

1. Bushnell, M. and Agrawal, V. D., Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic (2005).
2. Kropf, T., Introduction to Formal Hardware Verification, Springer Verlag (2001).

MMV-301.2 VLSI Architectures

L	T	P
3	1	0

UNIT-1 Complex Instruction Set Computers (CISC): Instruction Set, Characteristics and Functions, Addressing Modes, Instruction Formats, Architectural Overview, Processor Organization, Register Organization, Instruction Cycle, Instruction Pipelining, Pentium Processor, PowerPC Processor.

UNIT-2 Reduced Instruction Set Computers (RISC): Instruction execution Characteristics, Register Organization, Reduced Instruction Set, Addressing Modes, Instruction Formats, Architectural Overview, RISC Pipelining, Motorola 88510, MIPS R4650, RISC Vs. CISC.

UNIT-3 Pipeline Processing: Basic Concepts, Classification of Pipeline Processors, Instruction and Arithmetic Pipelining: Design of Pipelined Instruction Units, Pipelining Hazards and Scheduling, Principles of Designing Pipelined Processors.

UNIT-4 Memory Architectures: Memory hierarchy design, Multiprocessors, thread level parallelism and multi-core architectures, I/O buses. Arithmetic: Fixed point, Floating point and residue arithmetic, Multiply and Divide Algorithms.

UNIT-5 Issues in arithmetic system design, Issues in the applications (optimizing the hardware – software interface), ASIP, reconfigurable computing, Future microprocessor architectures. **Superscaler Processors**: Overview, Design Issues, PowerPC, Pentium.

Text Books:

1. Patterson, D. A. and Hennessy, J., Computer Architecture: A Quantitative Approach, Harcourt Asia (2003).
2. Stallings, W., Computer Organization and Architecture: Designing for Performance, Prentice Hall (2002).

Reference Books:

1. Patterson, D. A. and Hennessy, J., Computer Organization and Design, Harcourt Asia (1998).
2. Flynn, M. J. and Oberman, S. F., Advanced Computer Arithmetic Design, Wiley (2001).
3. Parhami, B., Computer Arithmetic Algorithms and Hardware Design, Oxford (2000).

MMV-301.3 NANOELECTRONICS

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UNIT-1 Shrink-down approaches: Introduction to Nanoscale Systems, Length energy and time scales, Top down approach to Nanolithography, CMOS Scaling, Limits to Scaling, System Integration Limits - Interconnect issues, *etc*. Overview of Nanoelectronics and Devices: The Nano-scale MOSFET, FinFETs, Vertical MOSFETs, Resonant Tunneling Transistors, Single Electron Transistors, New Storage devices, Optoelectronic and Spin electronics Devices.

UNIT-2 Basics of Quantum Mechanics: History of Quantum Mechanics, Schrödinger Equation, Quantum confinement of electrons in semiconductor nano structures, 2D confinement (Quantum Wells), Density of States, Ballistic Electron Transport, Coulomb Blockade, NEGF Formalism, Scattering.

UNIT-3 Leakage in Nanometer CMOS Technologies: Taxonomy of Leakage: Introduction, Sources, Impact and Solutions. Leakage dependence on Input Vector: Introduction, Stack Effect, Leakage reduction using Natural Stacks, Leakage reduction using Forced Stacks. Power Gating and Dynamic Voltage Scaling: Introduction, Power Gating, Dynamic Voltage Scaling, Power Gating methodologies.

UNIT-4 Nano-Fabrication and Characterization: Fabrication: Photolithography, Electron-beam Lithography, Advanced Nano-Lithography, Thin-Film Technology, MBE, CVD, PECVD. Characterization: Scanning Probe Microscopy, Electron Microscopy (TEM, SEM), Photon Spectroscopy, Nano Manipulators.

UNIT-5 Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Semiconductors and Metals, Electronic conduction in molecules, Molecular Logic Gates, Quantum point contacts, Quantum dots and Bottom up approach, Carbon Nano-tube and its applications, Quantum Computation and DNA Computation. Overview of Organic Electronics: OLEDs, OLETs, Organic Solar Cells.

Text Books:

1. Lundstorm, M. and Guo, J., Nanoscale Transistors – Device Physics, Modeling and Simulation, Springer (2006).
2. Bhushan, B., Handbook of Nanotechnology, 2nd Edition, Springer (2007).
3. Beenaker, C. W. J., and Houten, V., Quantum Transport in Semiconductor Nanostructures in Solid State Physics, Ehernreich and Turnbell, Academic Press (1991).

Reference Books:

1. Fahrner, W. R., Nanotechnology and Nanoelectronics: Materials, Devices and Measurement Techniques, Springer (2005).
2. Ferry, D., Transport in Nanostructures, Cambridge University Press (2000).
3. Mitin, V. V. and Kochelap, V. A., Introduction to Nanoelectronics: Science, Nanotechnology, Engineering and Application, Cambridge Press (2007).

4. Draoman, M. and Dragoman, D., Nanoelectronics: Principles and Devices, Artech House (2005).
5. Goddard, W., Brenner, D., Lyshevski, S. E. and Iafrate, G., Handbook of Nanoscience, Engineering and Technology, 2nd Edition, CRC Press (2007).
6. Lyshevski S. E., Molecular Electronics, Circuits, and Processing Platforms, CRC Press (2006).

MMV-302.1 MODELING TECHNIQUES FOR SUBMICRON DEVICES

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UNIT- 1 Semiconductor Fundamentals: Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, bandgap narrowing), Review of PN and MS diodes.

UNIT-2 Quantum Mechanics Fundamentals: Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling. Modeling and Simulation of Carrier Transport: Carrier Scattering (impurity, phonon, carrier- carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion.

UNIT-3 MOS Capacitors: Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).

UNIT-4 MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.

UNIT-5 Parameter Measurement: General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistors. Advanced Device Technology: SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling.

Text Books:

1. Sze, S. M., Physics of Semiconductor Devices, Wiley India Pvt. Ltd. (2008).
2. Tsividis, Y., Operation and Modeling of the MOS Transistor, Oxford University Press, (2008).
3. Taur, Y. and Ning, T. H., Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).

Reference Books:

1. Massobrio, G. and Antognetti, P., Semiconductor Device Modeling, McGraw-Hill (1998).
2. Dieter, K. S., Semiconductor Material and Device Characterization, John Wiley and Sons, (1990).
3. Muller, R. S., Kamins, T. I., and Chan, M., Device Electronics for Integrated Circuits, John Wiley and Sons (2002).
4. Tor, A., Fjeldly, T. Y., and Michael, S., Introduction to Device Modeling and Circuit Simulation, John Wiley and Sons (1998).

MMV-302.2 SYSTEM ON CHIP (SOC) DESIGN

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UNIT-1 Overview of SOC Design Process: Introduction, Top-down SOC design flow, Metrics of SOC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools..

UNIT-2 SOC Architecture Design: Introduction, Front-end chip design, Back-end chip design, Integration platforms and SOC.

UNIT-3 Design, Function Architecture Co-design, Designing Communication Networks, System Level Power Estimation and Modeling, Transaction Level Modeling, Design Space Exploration, Software design in SOCs.

UNIT-4 SOC Design and Test Optimization: Design methodologies for SOC, Noise and signal integrity analysis, System Integration issues for SOC, SOC Test Scheduling and Test Integration, SOC Test Resource partition.

Text Books:

1. Wolf, W., Modern VLSI Design: System-on-chip Design, 3rd Edition, Prentice Hall (2002).
2. Nekoogar, F. and Nekoogar, F., From ASICs to SOCs: A Practical Approach, 1st Edition, Prentice Hall (2003).
3. Uyemura, J. P., Modern VLSI Design – SOC Design, Prentice Hall (2001).
4. Lin, S. Y. L., Essential Issues in SOC Design: Designing Complex Systems-On-Chip, Springer (2004).

Reference Books:

1. Rajsuman, R., System-on-a-chip: Design and Test, Artech House (2000).
2. Nurmi, J., Tenhunen, H., Isoaho, J. and Jantsch, A., Interconnect-Centric Design for advanced SoC and NoC, Springer (2004).
3. Asheden, P. J. and Mermet J., System-on-Chip Methodologies and Design Languages, Kluwer Academic (2002).
4. Erbas, C., System-Level Modeling and Design Space Exploration for Multiprocessor Embedded System-on-Chip Architectures, Amsterdam University Press (2004).

MMV-302.3 HIGH SPEED VLSI DESIGN

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UNIT-1 Introduction of High Speed VLSI Circuits Design. Back-End-Of -Line variability considerations: Ideal and non ideal interconnect issues, Dielectric Thickness and Permittivity. The Method of Logical Effort: Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.

UNIT-2 Deriving the Method of Logical Effort: Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path , Using the wrong number of stages, Using the wrong gate size.

UNIT-3 Non-Clocked Logic Styles: Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Clocked Logic Styles: Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic.

UNIT-4 Circuit Design Margining: Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise. Latching Strategies: Basic Latch Design, Latching single-ended logic, Latching Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

UNIT-5 Interface Techniques: Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection. Clocking Styles: Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques. Skew Tolerant Design.

Text Books:

1. Bernstein, K., Carrig, K. M., Durham, Hansen, C. M., P. R., D., Hogenmiller, E. J., Nowak and N. J. Rohrer High Speed CMOS Design Styles, Kluwer (1998
2. Sutherland, I. E., Sproull, B. F. and Harris, D. L., Logical Effort: Designing Fast CMOS Circuits, Elsevier/MK (1999).

Reference Books:

1. Jhonson, H. W., High Speed Digital Design, Prentice Hall PTR (2008).